EAST SEARCH

6/19/2006

L#	Hits	Search String	Databases
S1	1254	((integrated or digital) near2 circuit$1) with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	59	S1 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	6387	circuit$1 with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	304	S3 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	304	S2 or S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	47	S5 and (reconfigurable with (logic or interconnect$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	127	S5 and (circuit with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	16	S5 and (circuit with partition$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	7	S5 and (on-board with processing$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	38	S5 and (element$1 with state$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	67	S5 and ((monitor$3 or report$3 or test$3) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	48	S5 and ((monitor$3 or report$3 or test$3) with command$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	27	S5 and (retriev$3 with state$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	93	S5 and ((analyz$3 or analysis) with data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	84	S5 and ((detect$3 or report$3) with event$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	87	S5 and (board with circuit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	10	S5 and (on-chip with processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	54	S5 and (local$2 with (monitor$3 or analyz$3 or analysis or report$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	30	S5 and (test$3 with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	38	S5 and ((generat$3 or produc$3) with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	3	S5 and (local$2 with (generat$3 or produc$3) with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	25	S5 and ((emulat$3 near2 system) with board$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	89	S5 and (workstation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	8	S5 and (EDA with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	167	S6 or S8 or S9 or S10 or S11 or S12 or S13 or S17 or S18 or S19 or S20 or S21 or S22 or S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	210	S7 or S14 or S15 or S16 or S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	133	S25 and S26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	167	S25 or S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	1254	((integrated or digital) near2 circuit$1) with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	59	S29 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	6387	circuit$1 with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	304	S31 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	304	S30 or S32	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	47	S33 and (reconfigurable with (logic or interconnect$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	127	S33 and (circuit with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	16	S33 and (circuit with partition$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	7	S33 and (on-board with processing$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S38	38	S33 and (element$1 with state$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	67	S33 and ((monitor$3 or report$3 or test$3) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	48	S33 and ((monitor$3 or report$3 or test$3) with command$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	27	S33 and (retriev$3 with state$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	93	S33 and ((analyz$3 or analysis) with data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	84	S33 and ((detect$3 or report$3) with event$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	87	S33 and (board with circuit$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	10	S33 and (on-chip with processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	54	S33 and (local$2 with (monitor$3 or analyz$3 or analysis or report$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	30	S33 and (test$3 with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	38	S33 and ((generat$3 or produc$3) with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	3	S33 and (local$2 with (generat$3 or produc$3) with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	25	S33 and ((emulat$3 near2 system) with board$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	89	S33 and (workstation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	8	S33 and (EDA with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	167	S34 or S36 or S37 or S38 or S39 or S40 or S41 or S45 or S46 or S47 or S48 or S49 or S50 o	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	210	S35 or S42 or S43 or S44 or S51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	133	S53 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	167	S53 or S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	4	6,265,894.pn. or "5,777,489".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	1318	((integrated or digital) near2 circuit$1) with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	62	S58 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	62	S58 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	6696	circuit$1 with emulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	321	S61 and (distributed with (emulat$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	321	S60 or S62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	50	S63 and (reconfigurable with (logic or interconnect$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	10	S63 and (on-chip with processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	32	S63 and (test$3 with (vector$1 or stimulus or stimulii))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	40	**S63 and ((generat$3 or produc$3) with (vector$1 or stimulus or stimulii))**	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	3	S63 and ((local$2 or on-chip) with (generat$3 or produc$3) with (vector$1 or stimulus or stimu	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	53	S65 or S66 or S67 or S68	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

10/003184 **Frederic Reblewski**

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6/19/2006

Results of search set S115

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050071716 A1	Testing of reconfigurable logic and interconnect sources	20050331	714/725	
US 20040260530 A1	Distributed configuration of integrated circuits in an emulation system	20041223	703/23	
US 20040220891 A1	Neural networks decoder	20041104	706/12	

US 20040181497 A1	Neural networks	20040916	706/23
US 20040078187 A1	Emulation components and system including distributed routing and configuration of emulatio	20040422	703/28
US 20040059876 A1	Real time emulation of coherence directories using global sparse directories	20040325	711/141
US 20040044514 A1	Polymorphic computational system and method in signals intelligence analysis	20040304	703/23
US 20040034841 A1	Emulation components and system including distributed event monitoring, and testing of an IC	20040219	716/8
US 20030233504 A1	Method for detecting bus contention from RTL description	20031218	710/107
US 20030149675 A1	Processing device with intuitive learning capability	20030807	706/2
US 20030105617 A1	Hardware acceleration system for logic simulation	20030605	703/14
US 20030074178 A1	Emulation system with time-multiplexed interconnect	20030417	703/25
US 20020177990 A1	Distributed logic analyzer for use in a hardware logic emulation system	20021128	703/28
US 20020161568 A1	Memory circuit for use in hardware emulation system	20021031	703/25
US 20020116168 A1	METHOD AND SYSTEM FOR DESIGN VERIFICATION OF ELECTRONIC CIRCUITS	20020822	703/28
US 20020066065 A1	Method, apparatus, and program for multiple clock domain partitioning through retiming	20020530	716/6
US 6922664 B1	Method and apparatus for multi-sensor processing	20050726	703/13
US 6920416 B1	Electronic systems testing employing embedded serial scan generator	20050719	703/13
US 6832178 B1	Method and apparatus for multi-sensor processing	20041214	702/189
US 6732068 B2	Memory circuit for use in hardware emulation system	20040504	703/24
US 6694464 B1	Method and apparatus for dynamically testing electrical interconnect	20040217	714/725
US 6684318 B2	Intermediate-grain reconfigurable processing device	20040127	712/15
US 6571370 B2	Method and system for design verification of electronic circuits	20030527	716/4
US 6567962 B2	Method, apparatus, and program for multiple clock domain partitioning through retiming	20030520	716/6
US 6496918 B1	Intermediate-grain reconfigurable processing device	20021217	712/15
US 6415188 B1	Method and apparatus for multi-sensor processing	20020702	700/67
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423	703/28
US RE37488 E	Heuristic processor	20011225	706/14
US 6266760 B1	Intermediate-grain reconfigurable processing device	20010724	712/15
US 6052524 A	System and method for simulation of integrated hardware and software components	20000418	703/22
US 5960191 A	Emulation system with time-multiplexed interconnect	19990928	703/28
US 5956518 A	Intermediate-grain reconfigurable processing device	19990921	712/15
US 5943490 A	Distributed logic analyzer for use in a hardware logic emulation system	19990824	703/28
US 5940603 A	Method and apparatus for emulating multi-ported memory circuits	19990817	716/5
US 5937154 A	Manufacturing functional testing of computing devices using microprogram based functional te	19990810	714/30
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5838948 A	System and method for simulation of computer systems combining hardware and software int	19981117	703/27
US 5761077 A	Graph partitioning engine based on programmable gate arrays	19980602	716/7
US 5684721 A	Electronic systems and emulation and testing devices, cables, systems and methods	19971104	703/23
US 5663900 A	Electronic simulation and emulation system	19970902	
US 5621651 A	Emulation devices, systems and methods with distributed control of test interfaces in clock do	19970415	703/23
US 5517597 A	Convolutional expert neural system (ConExNS)	19960514	706/26
US 5475793 A	Heuristic digital processor using non-linear transformation	19951212	706/14
US 5452239 A	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implemen	19950919	703/19
US 5377306 A	Heuristic processor	19941227	706/14
US 5357597 A	Convolutional expert neural system (ConExNS)	19941018	706/25
US 5222193 A	Training system for neural networks and the like	19930622	706/25

US 5113500 A	Multiple cooperating and concurrently operating processors using individually dedicated mem	19920512	710/305
US 5087826 A	Multi-layer neural network employing multiplexed output neurons	19920211	706/38
US 4961002 A	Synapse cell employing dual gate transistor structure	19901002	365/185.03
US 4896053 A	Solitary wave circuit for neural network emulation	19900123	706/38
US 4802103 A	Brain learning and recognition emulation circuitry and method of recognizing events	19890131	706/38
US 4773024 A	Brain emulation circuit with reduced confusion	19880920	706/20

Interference checked

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L#	Hits	Search String	Databases
S75	386	((integrated or digital) near2 circuit$1) with emulat$3	US-PGPUB
S76	27	S75 and (distributed with (emulat$3 or processing))	US-PGPUB
S77	3	S76 and (on-chip with processing)	US-PGPUB
S78	3	S77 and (on-chip.CLM.)	US-PGPUB

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US 20040181497 A1	Neural networks	20040916	706/23	
US 20040078187 A1	Emulation components and system including distributed routing and configuration of emulatic	20040422	703/28	
US 20040059876 A1	Real time emulation of coherence directories using global sparse directories	20040325	711/141	
US 20040044514 A1	Polymorphic computational system and method in signals intelligence analysis	20040304	703/23	
US 20040034841 A1	Emulation components and system including distributed event monitoring, and testing of an I	20040219	716/8	
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US 20030149675 A1	Processing device with intuitive learning capability	20030807	706/2	
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US 20020116168 A1	METHOD AND SYSTEM FOR DESIGN VERIFICATION OF ELECTRONIC CIRCUITS	20020822	703/28	
US 20020066065 A1	Method, apparatus, and program for multiple clock domain partitioning through retiming	20020530	716/6	
US 6922664 B1	Method and apparatus for multi-sensor processing	20050726	703/13	
US 6920416 B1	Electronic systems testing employing embedded serial scan generator	20050719	703/13	
US 6832178 B1	Method and apparatus for multi-sensor processing	20041214	702/189	
US 6732068 B2	Memory circuit for use in hardware emulation system	20040504	703/24	
US 6694464 B1	Method and apparatus for dynamically testing electrical interconnect	20040217	714/725	
US 6684318 B2	Intermediate-grain reconfigurable processing device	20040127	712/15	

US 6571370 B2	Method and system for design verification of electronic circuits	20030527	716/4
US 6567962 B2	Method, apparatus, and program for multiple clock domain partitioning through retiming	20030520	716/6
US 6496918 B1	Intermediate-grain reconfigurable processing device	20021217	712/15
US 6415188 B1	Method and apparatus for multi-sensor processing	20020702	700/67
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423	703/28
US RE37488 E	Heuristic processor	20011225	706/14
US 6266760 B1	Intermediate-grain reconfigurable processing device	20010724	712/15
US 6052524 A	System and method for simulation of integrated hardware and software components	20000418	703/22
US 5960191 A	Emulation system with time-multiplexed interconnect	19990928	703/28
US 5956518 A	Intermediate-grain reconfigurable processing device	19990921	712/15
US 5943490 A	Distributed logic analyzer for use in a hardware logic emulation system	19990824	703/28
US 5940603 A	Method and apparatus for emulating multi-ported memory circuits	19990817	716/5
US 5937154 A	Manufacturing functional testing of computing devices using microprogram based functional t	19990810	714/30
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5838948 A	System and method for simulation of computer systems combining hardware and software in	19981117	703/27
US 5761077 A	Graph partitioning engine based on programmable gate arrays	19980602	716/7
US 5684721 A	Electronic systems and emulation and testing devices, cables, systems and methods	19971104	703/23
US 5663900 A	Electronic simulation and emulation system	19970902	
US 5621651 A	Emulation devices, systems and methods with distributed control of test interfaces in clock dc	19970415	703/23
US 5517597 A	Convolutional expert neural system (ConExNS)	19960514	706/26
US 5475793 A	Heuristic digital processor using non-linear transformation	19951212	706/14
US 5452239 A	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implemer	19950919	703/19
US 5377306 A	Heuristic processor	19941227	706/14
US 5357597 A	Convolutional expert neural system (ConExNS)	19941018	706/25
US 5222193 A	Training system for neural networks and the like	19930622	706/25
US 5113500 A	Multiple cooperating and concurrently operating processors using individually dedicated mem	19920512	710/305
US 5087826 A	Multi-layer neural network employing multiplexed output neurons	19920211	706/38
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